

## **Introduction**

Lattice Semiconductor Corporation, the pioneer of non-volatile E<sup>2</sup>CMOS<sup>®</sup> in-system programmable (ISP<sup>™</sup>) logic, has now expanded the application of ISP PLDs to include programmable switching, interconnect and jumper functions with the ispGDX and the ispGDS devices. In-system programmability allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

The ispGDXV and ispGDX families provide designers with programmable alternatives for integration of eight- and 16-bit interface functions, as well as high performance and flexibility in system-level signal routing and interface applications.

This ispGDS (Generic Digital Switch) Family is an innovative programmable switch matrix architecture that allows quick implementation of changes to PCB connections without changing mechanical switches or other system hardware.

The ispGDXV, ispGDX and ispGDS devices provide higher quality and reliability than other interface and switch solutions due to the nature of E<sup>2</sup>CMOS technology. E<sup>2</sup>CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate design modifications. This same capability allows full parametric testability during manufacturing which guarantees 100 percent programming and functional yield.

The ispGDX Development System supports ispGDXV and ispGDX design using a simple language syntax from its own Graphical User Interface (GUI), called Design Manager. From creation to in-system programming, the ispGDX Development System is an easy-to-use, self-contained design tool.

The ispGDS Compiler is a simple DOS command line compiler which accepts an ASCII text file of the ispGDS design description and produces a JEDEC file for programming and a .doc file containing design compilation details. The ispGDS Compiler syntax is easy, yet powerful, allowing the use of labels and operators.

### **ispGDXV Family**

- ☐ Flexible Architecture
- ☐ 3.3V Core Voltage
- ☐ Programmable 3.3V or 2.5V Output Levels

- ☐ 250MHz System Performance
- ☐ 3.5ns Pin-to-Pin Delay
- ☐ 80 to 240 Programmable I/O Pins
- ☐ Programmable Wide MUX Supports up to 16:1 MUX
- ☐ Boundary Scan Test (IEEE 1149.1 Standard)
- ☐ PCI Compatible Output Drive

### **ispGDX Family**

- ☐ Flexible Architecture, 5V Core Voltage
- ☐ 111MHz System Performance
- ☐ 5ns Pin-to-Pin Delay
- ☐ 80 to 160 Programmable I/O Pins
- ☐ Boundary Scan Test (IEEE 1149.1 Standard)
- ☐ PCI Compatible 24mA Output Drive
- ☐ Lattice ISP or ispJTAG<sup>™</sup> Programming Interface

### **ispGDS Family**

- ☐ High-Speed Switch Matrix
- ☐ 7.5ns Propagation Delay
- ☐ 14, 18, or 22 I/Os
- ☐ In-System Programmable

### **ISP Product Technology**

- ☐ UltraMOS E<sup>2</sup>CMOS — the PLD Technology of Choice
- ☐ Electrically Erasable/Programmable/Reprogrammable
- ☐ 100% Tested During Manufacture
- ☐ 100% Programming Yield
- ☐ Fast Programming

### **ispGDX Development System Software**

- ☐ Easy-to-use Text Entry System
- ☐ Industry Standard JEDEC File for Programming
- ☐ Min / Max and Detailed Timing Reports
- ☐ Interfaces to Popular Timing Simulators
- ☐ Detailed Log and Report Files for Easy Design Debug
- ☐ On-line Help
- ☐ Windows<sup>®</sup> 98, Windows 95 and Windows NT<sup>®</sup> Compatible Graphical User Interface
- ☐ Solaris and HP-UX, Command Line Driven Version Available

# Introduction to ispGD XV, ispGD X and ispGD S Families

## ispGD S Compiler

- ❑ Accepts ASCII Text Design Description
- ❑ Includes Preprocessor For Adding Labels and Inversion
- ❑ Industry Standard JEDEC File for Programming

## ispGD XV and ispGD X Family Overview

The Generic Digital Crosspoint families (ispGD X and ispGD XV) from Lattice Semiconductor consists of seven members, ranging from 80 to 240 programmable I/Os. This innovative in-system programmable architecture has been optimized for digital signal interface and routing applications and features a series of special-purpose programmable I/O cells interconnected by an E<sup>2</sup>CMOS Global Routing Pool (GRP).

Any input can be routed to any output and each I/O cell has individual programmable I/O tri-state control (OE), output latch clock (CLK), programmable polarity, open-drain output emulation and two MUX select (MUXsel) inputs which control a fast 4:1 MUX allowing dynamic selection of up to four signal sources for a given output. Inputs or outputs can be combinatorial, latched, registered or driven to a static HIGH or LOW state.

The 3.3V ispGD XV Family is a functional superset of the ispGD X family, adding new features and greater I/O options. The I/Os are capable of 3.3V and 2.5V input/output levels.

High performance (3.5ns) in this family is combined with low power in space-saving BGA, TQFP and PQFP packages.

## ispGD S Family Overview

The ispGD S (Generic Digital Switch) Family combines the in-system programmability, high performance and low power of Lattice Semiconductor's GAL programmable logic technology with a switch matrix architecture, resulting in an innovative programmable signal router. The ispGD S is a configurable switch matrix which provides the ability to quickly implement and change PCB connections without changing mechanical switches or other system hardware. ISP allows the connections to be reprogrammed without removal from the printed circuit board via a simple 5V, 4-wire serial interface. This capability allows the system designer to define hardware which can be reconfigured in-system to meet a variety of applications. The ispGD S also conserves board real estate, providing up to 22 I/Os in about a quarter square inch of board space.

With today's demand for user-friendly systems, there is an increasing need for hardware which is easily reconfigured under software control without manual intervention. The ispGD S family is an ideal solution for end-system feature reconfiguration and signal routing applications. The fast 7.5ns propagation delay through the devices supports high-performance signal routing applications. Easier system upgrades, user feature selection and system manufacturing are the results.

There are three members of the ispGD S Family: the ispGD S22, ispGD S18 and ispGD S14. Each of the devices operate identically with the only difference being the number of I/O cells available.

**Table 1. ispGD X/V Family Attributes**

	ispGD X80A/VA	ispGD X120A	ispGD X160A/VA	ispGD X240VA
Voltage	5V/3.3V	5V	5V/3.3V	3.3V
I/O Pins	80	120	160	240
Speed: f <sub>max</sub> (MHz)*	143/250	143	143/250	167
Speed: t <sub>pd</sub> (ns)	5/3.5	5	5/3.5	5/4.5
Dedicated Clock Pins	2	4	4	4
Pin/Packages	100-Pin TQFP	160-Pin PQFP 176-Pin TQFP	208-Pin PQFP 208-Ball fpBGA 272-Ball BGA	388-Pin fpBGA

\*f<sub>max</sub> = 1/(t<sub>wh</sub> + t<sub>wl</sub>)

GD X Attributes

# Introduction to ispGD XV, ispGD X and ispGDS Families

Figure 1. ispGD XV and ispGD X Family Packages

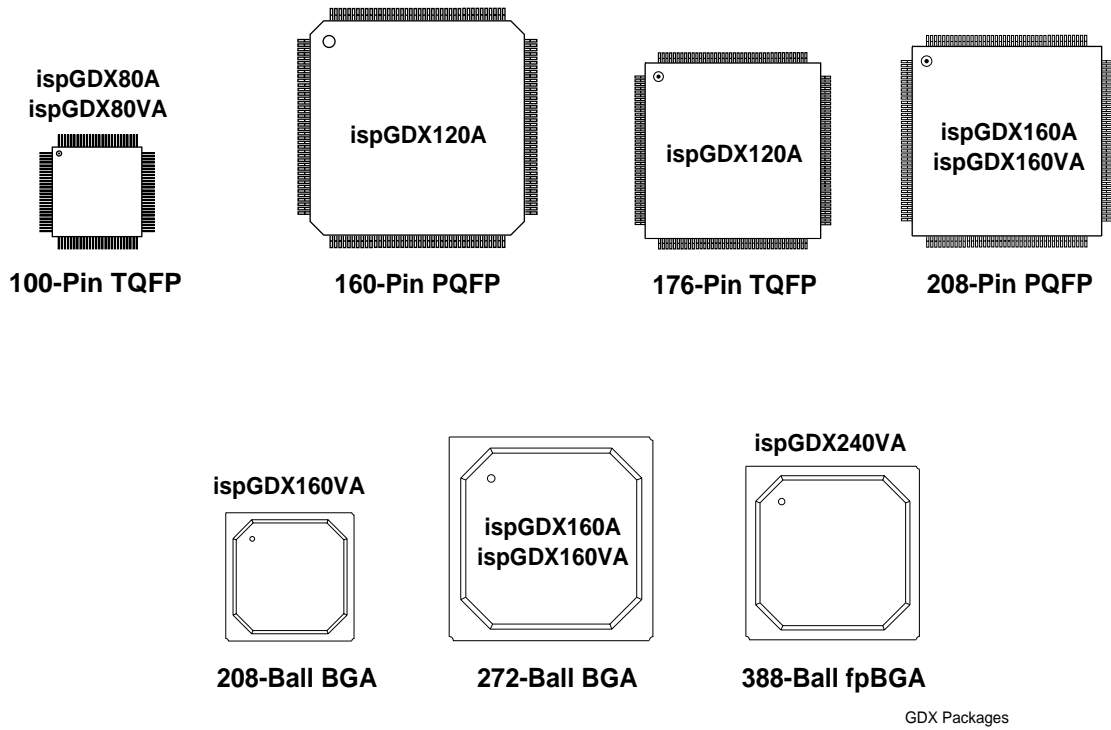


Figure 2. ispGDS Family Packages

