ispGAL22V10

In-System Programmable E²CMOS PLD
Generic Array Logic™

FEATURES

- **IN-SYSTEM PROGRAMMABLE™ (5-V ONLY)**
  - **— 4-Wire Serial Programming Interface**
  - **— Minimum 10,000 Program/Erase Cycles**
  - **— Built-in Pull-Down on SDI Pin Eliminates Discrete Resistor on Board (ispGAL22V10C Only)**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Fmax = 111 MHz**
  - **— 5 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL LOGIC INPUT AND I/O PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and CMOS 22V10 Devices**
- **E² CELL TECHNOLOGY**
  - **— In-System Programmable Logic**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Software-Driven Hardware Configuration**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

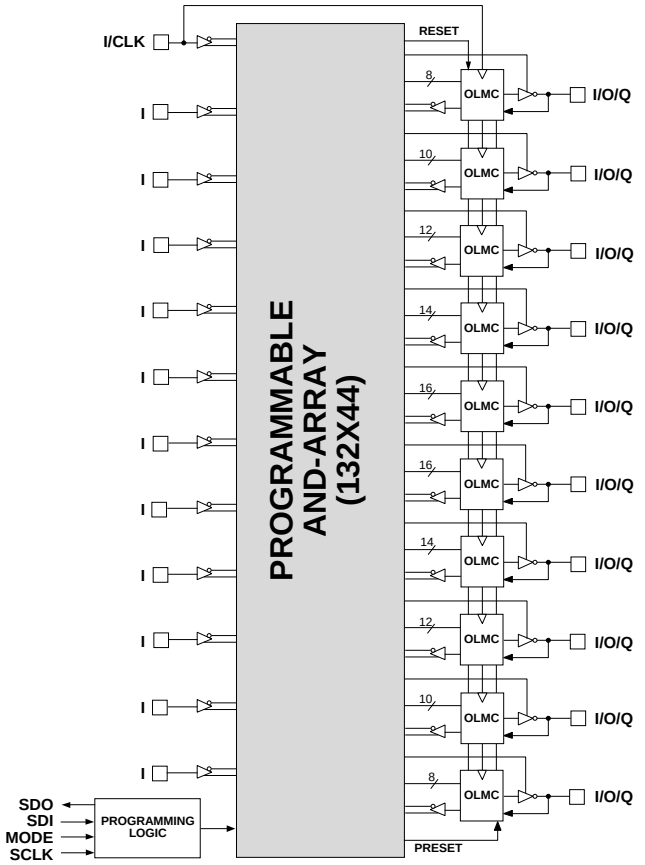
DESCRIPTION

The ispGAL22V10, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the industry's first in-system programmable 22V10 device. E^2 technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The ispGAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices. The standard PLCC package provides the same functional pinout as the standard 22V10 PLCC package with No-Connect pins being used for the ISP interface signals.

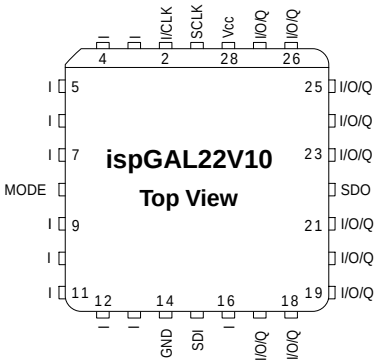
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 10,000 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

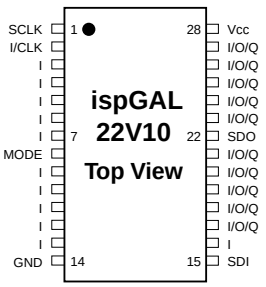


PIN CONFIGURATION

PLCC



SSOP



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1996 Data Book

ORDERING INFORMATION

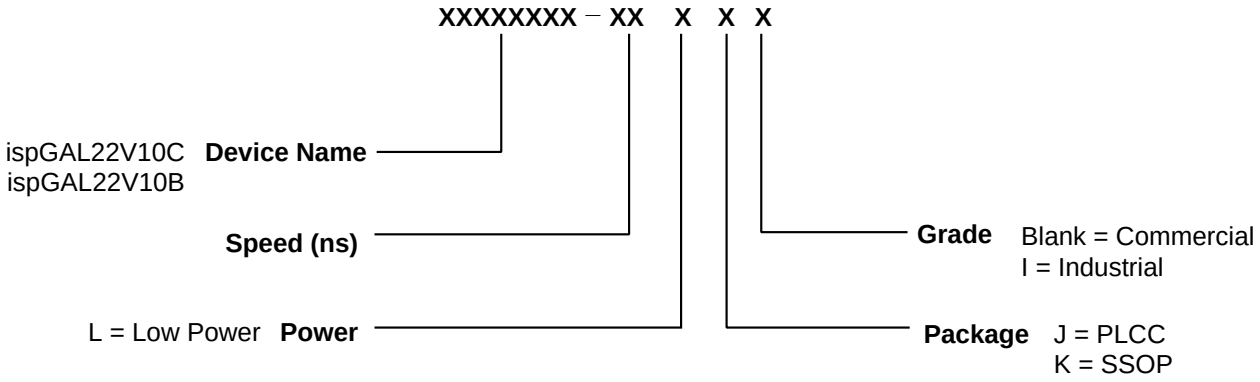
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	6.5	5	140	ispGAL22V10C-7LJ	28-Lead PLCC
				ispGAL22V10C-7LK	28-Lead SSOP
				ispGAL22V10B-7LJ	28-Lead PLCC
10	7	7	140	ispGAL22V10C-10LJ	28-Lead PLCC
				ispGAL22V10C-10LK	28-Lead SSOP
				ispGAL22V10B-10LJ	28-Lead PLCC
15	10	8	140	ispGAL22V10C-15LJ	28-Lead PLCC
				ispGAL22V10C-15LK	28-Lead SSOP
				ispGAL22V10B-15LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	8	165	ispGAL22V10C-15LJI	28-Lead PLCC
				ispGAL22V10C-15LKI	28-Lead SSOP

PART NUMBER DESCRIPTION



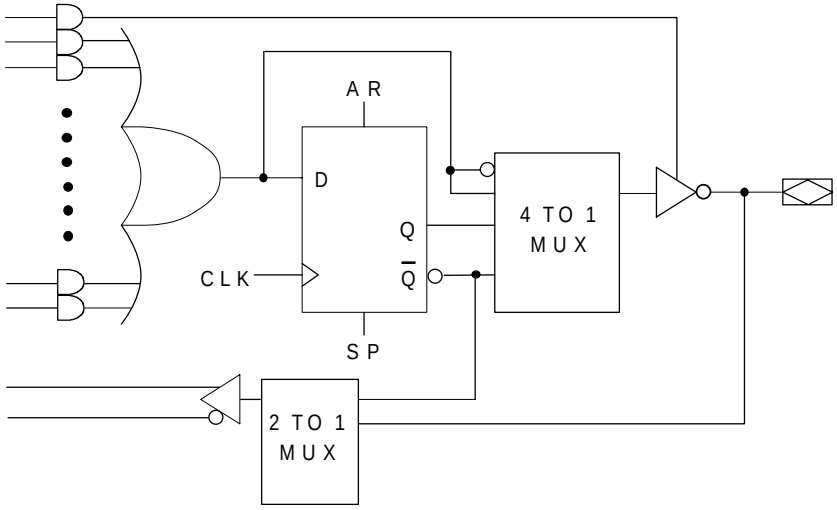
OUTPUT LOGIC MACROCELL (OLMC)

The ispGAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The ispGAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



ispGAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the ispGAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

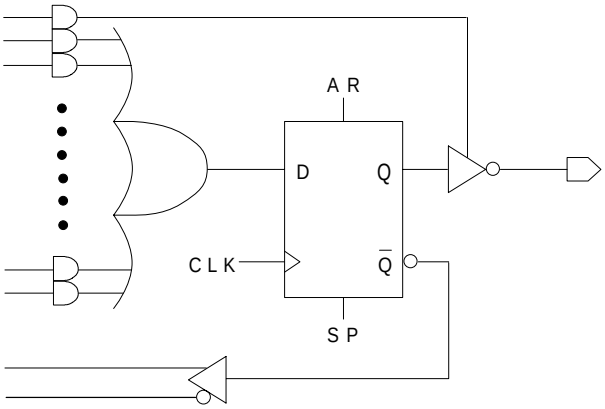
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

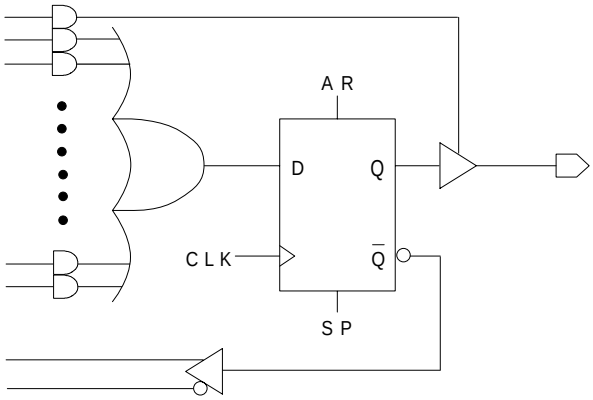
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

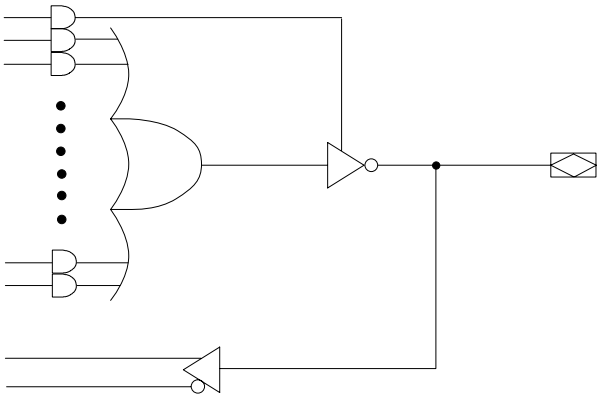
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

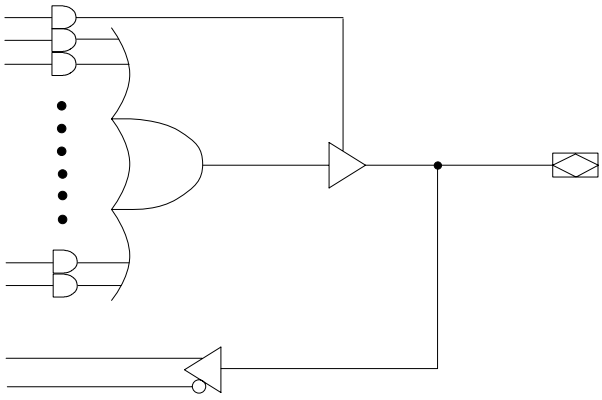
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

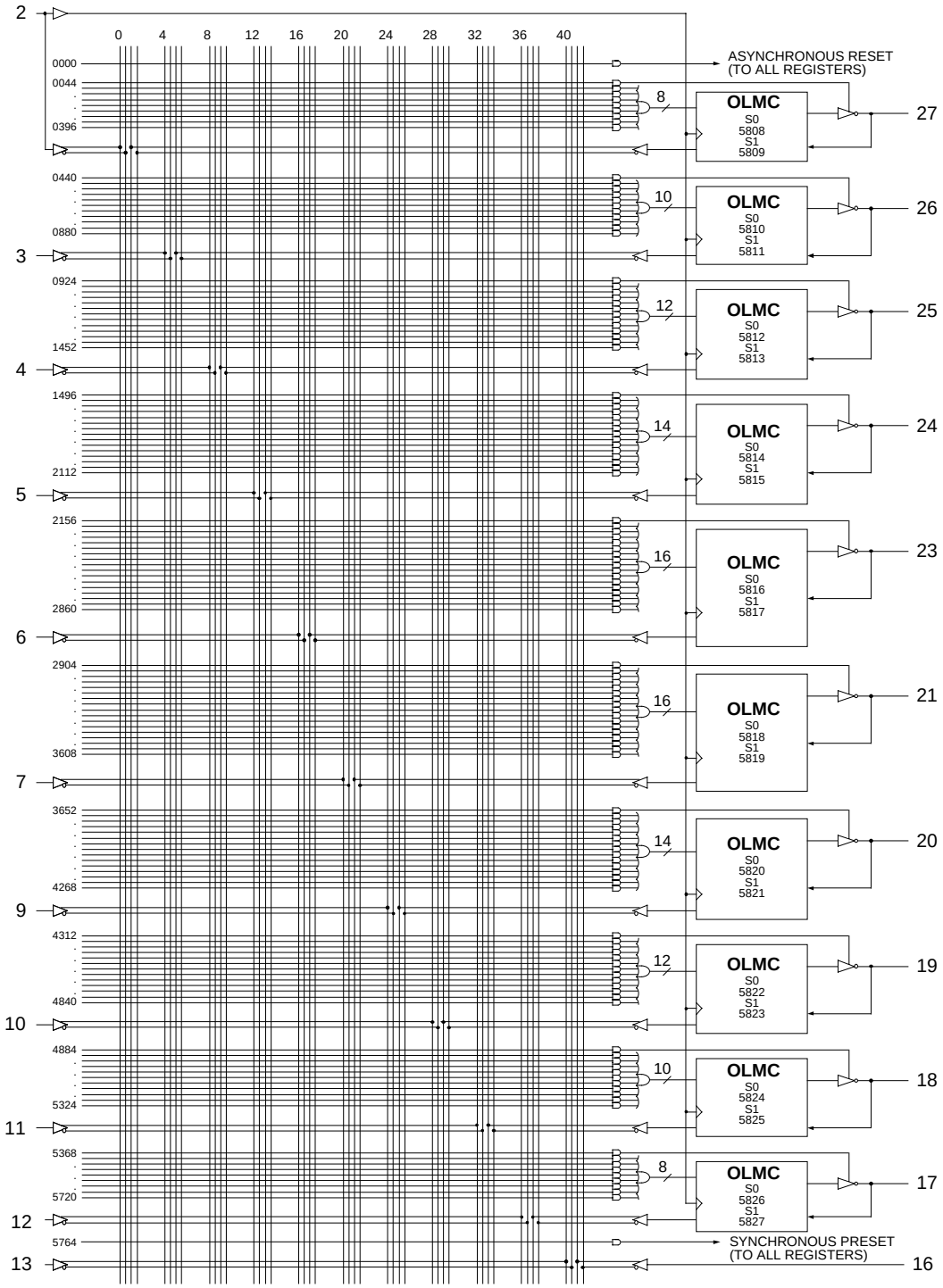


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

ispGAL22V10 LOGIC DIAGRAM / JEDEC FUSE MAP

PLCC & SSOP Package Pinout



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB