ispGAL®22LV10

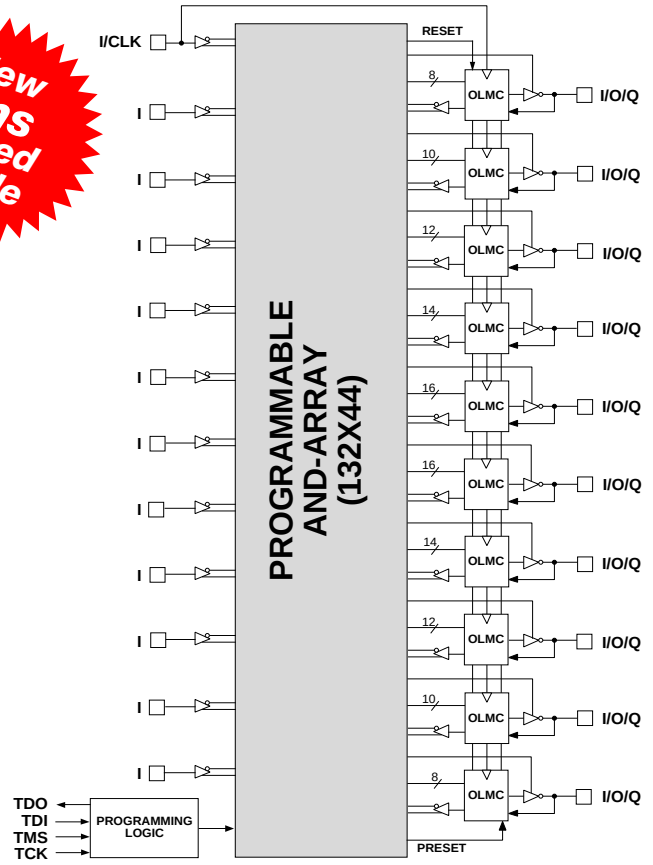
In-System Programmable Low Voltage E²CMOS® PLD Generic Array Logic™

Features

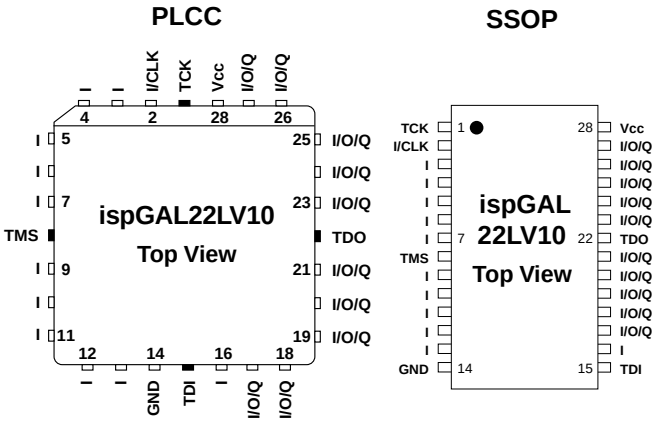
- **IN-SYSTEM PROGRAMMABLE**
  - — IEEE 1149.1 Standard TAP Controller Port Programming
  - — 4-Wire Serial Programming Interface
  - — Minimum 10,000 Program/Erase Cycles
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — 4 ns Maximum Propagation Delay
  - — Fmax = 250 MHz
  - — 3 ns Maximum from Clock Input to Data Output
  - — UltraMOS® Advanced CMOS Technology
- **3.3V LOW VOLTAGE 22V10 ARCHITECTURE**
  - — JEDEC-Compatible 3.3V Interface Standard
  - — 5V Tolerant Inputs and I/O
  - — I/O Interfaces with Standard 5V TTL Devices
- **ACTIVE PULL-UPS ON ALL LOGIC INPUT AND I/O PINS**
- **COMPATIBLE WITH STANDARD 22LV10/22V10 DEVICES**
  - — Function/Fuse-Map Compatible with 22LV10/22V10 Devices
  - — Parametric Compatible with 22LV10
- **E² CELL TECHNOLOGY**
  - — In-System Programmable Logic
  - — 100% Tested/100% Yields
  - — High Speed Electrical Erasure (<100ms)
  - — 20 Year Data Retention
- **APPLICATIONS INCLUDE:**
  - — DMA Control
  - — State Machine Control
  - — High Speed Graphics Processing
  - — Software-Driven Hardware Configuration
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

New 4ns Speed Grade

Functional Block Diagram



Pin Configuration



Description

The ispGAL22LV10 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. The ispGAL22LV10 can interface with both 3.3V and 5V signal levels.

The ispGAL22LV10 is fully function/fuse map compatible with the GAL®22LV10 and GAL22V10. Further, the ispGAL22LV10 is parametric compatible with the GAL22LV10. The ispGAL22LV10 also shares the same 28-pin PLCC package pin-out as the GAL22LV10.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 10,000 erase/write cycles and data retention in excess of 20 years are specified.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
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December 1999

Ordering Information

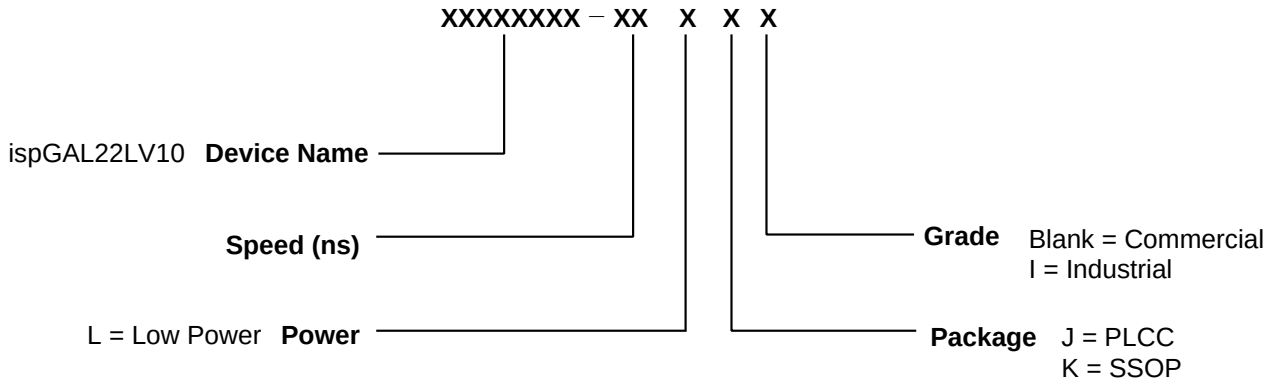
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	3	3	130	ispGAL22LV10-4LJ	28-Lead PLCC
				ispGAL22LV10-4LK	28-Lead SSOP
5	3.5	3.5	130	ispGAL22LV10-5LJ	28-Lead PLCC
				ispGAL22LV10-5LK	28-Lead SSOP
7.5	5	5	130	ispGAL22LV10-7LJ	28-Lead PLCC
				ispGAL22LV10-7LK	28-Lead SSOP
10	7	6.5	130	ispGAL22LV10-10LJ	28-Lead PLCC
				ispGAL22LV10-10LK	28-Lead SSOP
15	10	8	130	ispGAL22LV10-15LJ	28-Lead PLCC
				ispGAL22LV10-15LK	28-Lead SSOP

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	5	5	160	ispGAL22LV10-7LJI	28-Lead PLCC
				ispGAL22LV10-7LKI	28-Lead SSOP
10	7	6.5	160	ispGAL22LV10-10LJI	28-Lead PLCC
				ispGAL22LV10-10LKI	28-Lead SSOP
15	10	8	160	ispGAL22LV10-15LJI	28-Lead PLCC
				ispGAL22LV10-15LKI	28-Lead SSOP

Part Number Description



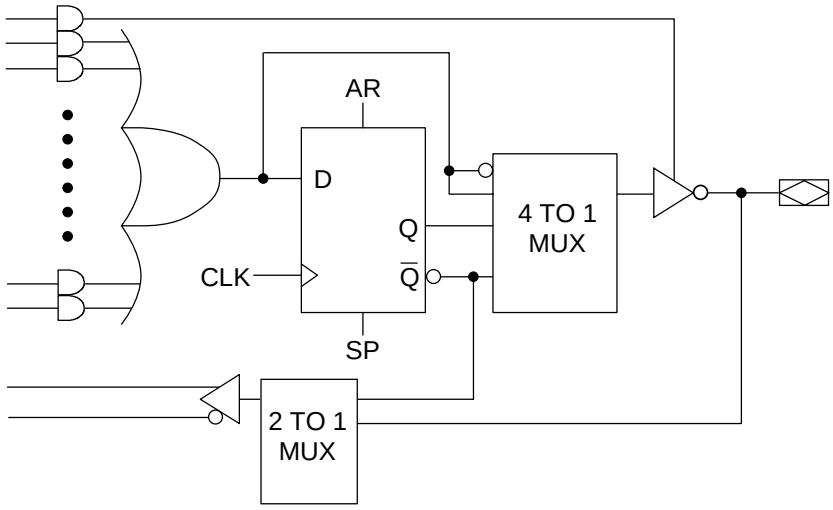
Output Logic Macrocell (OLMC)

The ispGAL22LV10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The ispGAL22LV10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



ispGAL22LV10 OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the ispGAL22LV10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (S0 and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

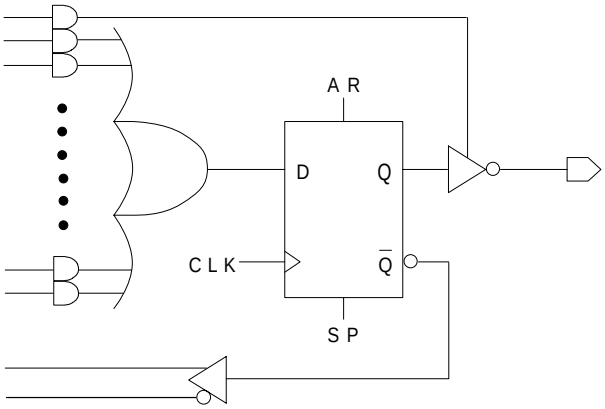
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

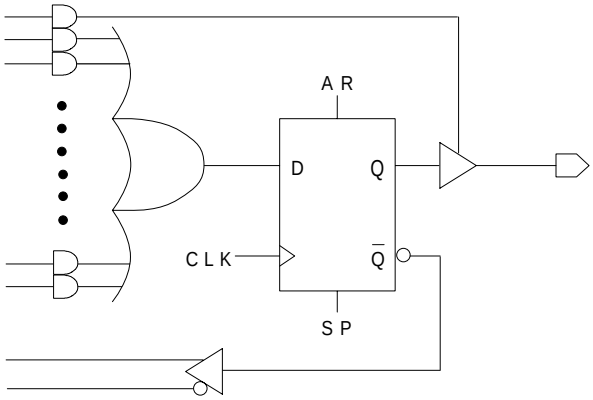
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

Registered Mode



ACTIVE LOW

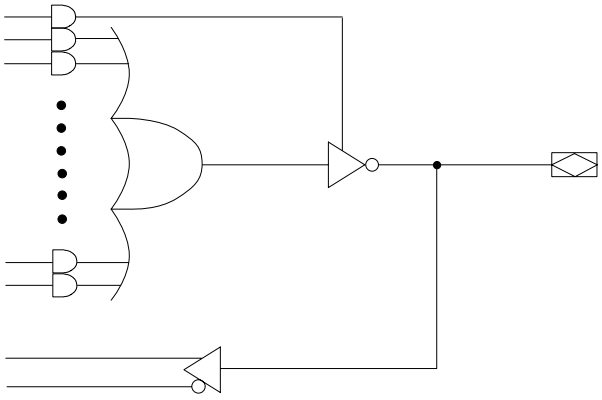
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

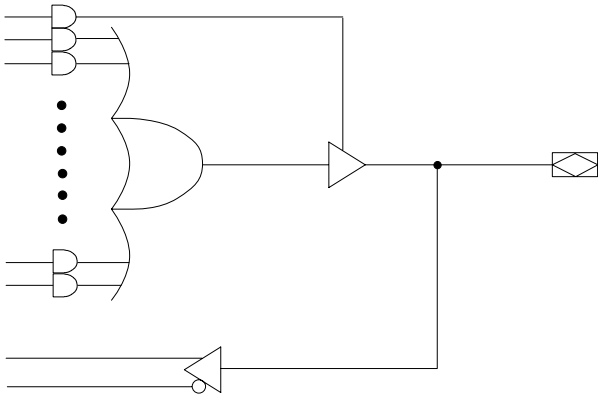
$S_0 = 1$
$S_1 = 0$

Combinatorial Mode



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

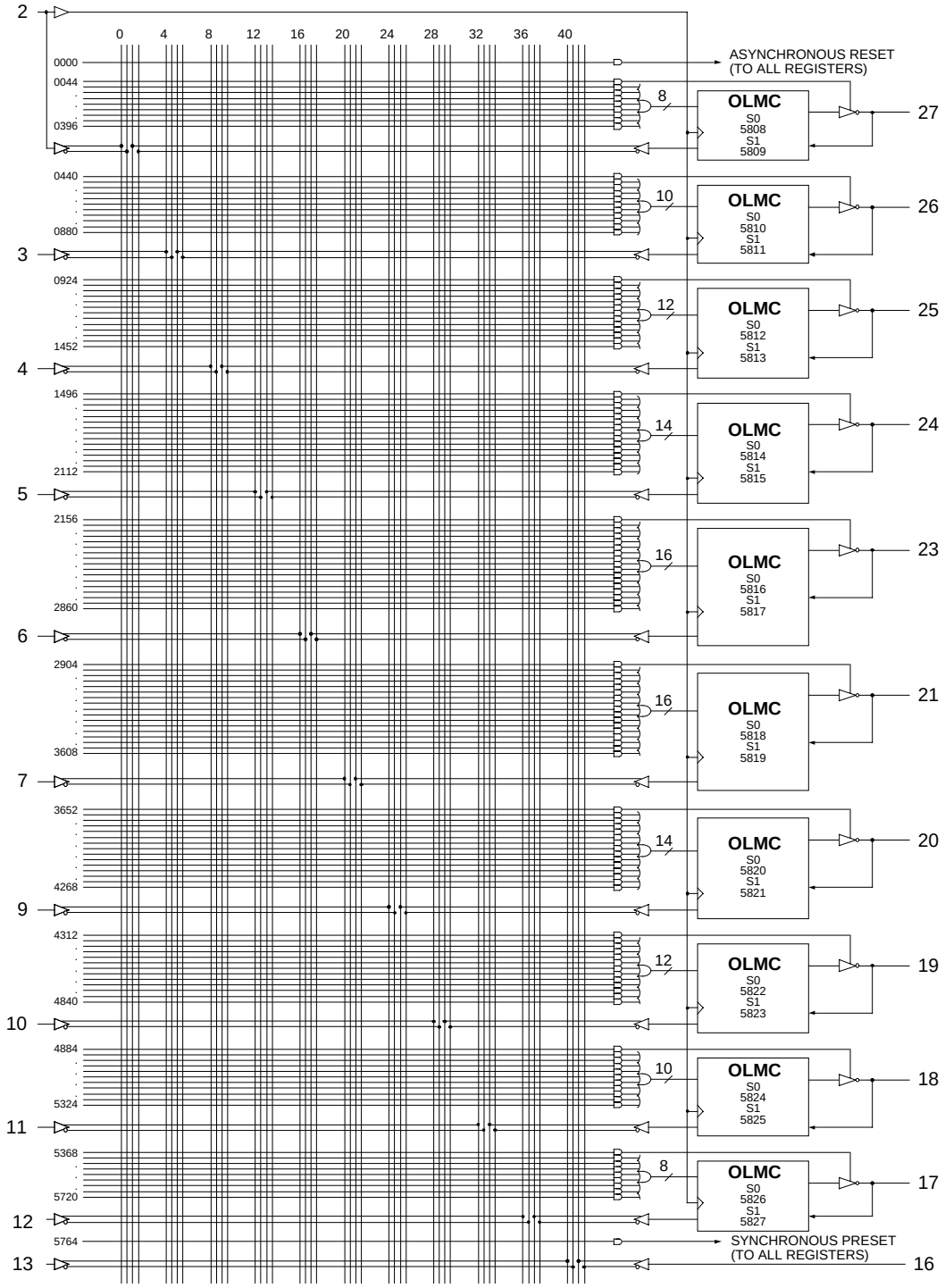


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

ispGAL22LV10 Logic Diagram/JEDEC Fuse Map

PLCC & SSOP Package Pinout



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB