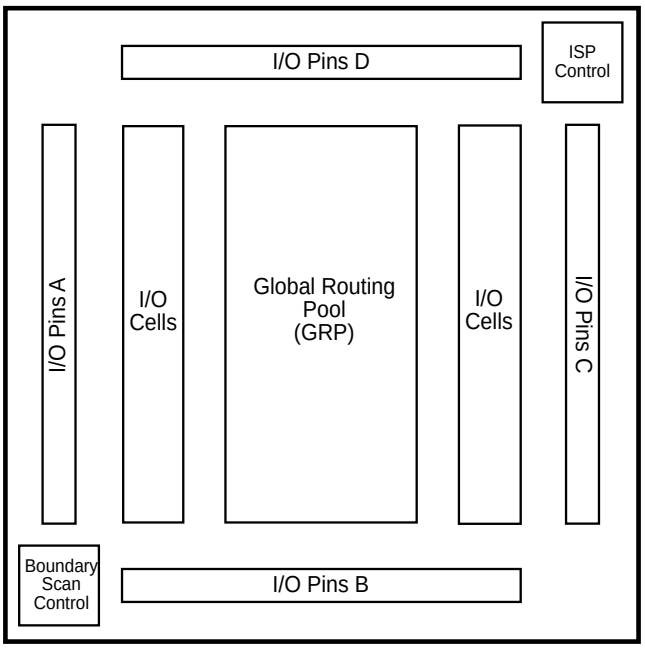
ispGDX™ Family

In-System Programmable Generic Digital Crosspoint™

Features

- **IN-SYSTEM PROGRAMMABLE GENERIC DIGITAL CROSSPOINT FAMILY**
  - **— Advanced Architecture Addresses Programmable PCB Interconnect, Bus Interface Integration and Jumper/Switch Replacement**
  - **— Three Device Options: 80 to 160 Programmable I/O Pins**
  - **— "Any Input to Any Output" Routing**
  - **— Fixed HIGH or LOW Output Option for Jumper/DIP Switch Emulation**
  - **— Space-Saving TQFP, PQFP and BGA Packaging**
  - **— Dedicated IEEE 1149.1-Compliant Boundary Scan Test**
  - **— PCI Compliant Output Drive**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 5V Power Supply**
  - **— 5.0ns Input-to-Output/5.0ns Clock-to-Output Delay**
  - **— Low-Power: 40mA Quiescent Icc**
  - **— Balanced 24mA Output Buffers with Programmable Slew Rate Control**
  - **— Schmitt Trigger Inputs for Noise Immunity**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested**
- **ispGDX OFFERS THE FOLLOWING ADVANTAGES**
  - **— In-System Programmable**
  - **— Lattice ISP or JTAG Programming Interface**
  - **— Only 5V Power Supply Required**
  - **— Change Interconnects in Seconds**
  - **— Reprogram Soldered Devices**
- **FLEXIBLE ARCHITECTURE**
  - **— Combinatorial/Latched/Registered Inputs or Outputs**
  - **— Individual I/O Tri-state Control with Polarity Control**
  - **— Dedicated Clock Input Pins (two or four) or Programmable Clocks from I/O Pins (from 20 up to 40)**
  - **— Up to 4:1 Dynamic Path Selection**
  - **— Programmable Output Pull-up Resistors**
  - **— Outputs Tri-state During Power-up ("Live Insertion" Friendly)**
- **DESIGN SUPPORT THROUGH LATTICE'S ispGDX DEVELOPMENT SOFTWARE**
  - **— MS Windows or NT / PC-Based or Sun O/S**
  - **— Easy Text-Based Design Entry**
  - **— Automatic Signal Routing**
  - **— Program up to 100 ISP Devices Concurrently**
  - **— Simulator Netlist Generation for Easy Board-Level Simulation**

Functional Block Diagram



Description

The ispGDX architecture provides a family of fast, flexible programmable devices to address a variety of system-level digital signal routing and interface requirements including:

- Multi-Port Multiprocessor Interfaces
- Wide Data and Address Bus Multiplexing (e.g. 4:1 High-Speed Bus MUX)
- Programmable Control Signal Routing (e.g. Interrupts, DMAREQs, etc)
- Board-Level PCB Signal Routing for Prototyping or Programmable Bus Interfaces

The ispGDX Family consists of three members with 80, 120 and 160 Programmable I/Os. These devices are available in packages ranging from the 100-pin TQFP to the 208-pin PQFP. The devices feature fast operation, with input-to-output signal delays (Tpd) of 5ns and clock-to-output delays of 5ns.

The architecture of the devices consists of a series of programmable I/O cells interconnected by a Global Rout-

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